



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shuichi Kikuchi et al.

Art Unit : 2814

Serial No. : 09/444,819

Examiner : S. Rao

Filed : November 22, 1999

Title : SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

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Commissioner for Patents

Washington, D.C. 20231

RESPONSE

Claims 1 to 4, 8 to 10, 17, and 19 are pending.

Claims 1 and 2 have been rejected as being anticipated by Bulucea. However, it is submitted that claims 1 and 2 are not anticipated by Bulucea.

Discussion Regarding Claim 1

On page 3 of the outstanding office action, it is alleged that Bulucea discloses "a drift region (Fig. 13, #136; col. 20, line 7) adjacent to the channel region and extending to and below the drain region, wherein the drift region (136) is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region (Fig. 13)." However, claim 1 is not anticipated by the cited prior art for the following reasons.

Bulucea does not disclose the drift region as claimed in claim 1. First, the lightly doped extension 136, which the Examiner equates with the present invention's drift region, is not a drift region but a drain region. In column 20, lines 4 to 6, Bulucea states referring to Fig. 13 that "the FET 130 has ... a drain zone formed with n++ main portion 135 and more lightly doped n+

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